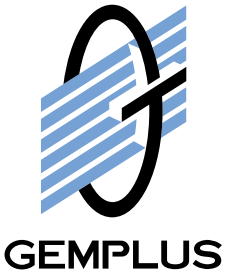
GemCore Serial Lite PRO

Technical Specifications



GEMPLUS, B.P. 100, 13881 GEMENOS CEDEX, FRANCE.

Tel: +33 (0)4.42.36.50.00 Fax: +33 (0)4.42.36.50.90

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Introduction

This document provides information about the GemCore™ Serial Lite PRO (GSLP) chip, and in particular about its hardware characteristics and performances. A typical smart card reader diagram is also provided with integration guidelines. The description of the product operating mode is given in the document "*GemCore Serial Lite PRO V1.4 Reference Manual*".

Who Should Read This Book

This document is intended for electronics engineers.

Contacting our Hotline

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Corporate and EMEA

Hotline: +33 (0)4 42 36 50 50

Hot Fax: +33 (0)4 42 36 50 98

Email: hotline@gemplus.com

Americas

Hotline: 1 (877) 436-7233

Hot Fax: 1 (215) 390-1586

Email: hotlineusa@gemplus.com

From our Web Site

http://www.gemplus.com

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GemCore Serial Lite PRO Technical Features

General Description

GemCore Serial Lite PRO is designed to simplify the integration of smart card interfaces in electronic devices.

It manages the electrical interface and communication with ISO 7816 –1/2/3/4 compatible smart cards and memory cards.

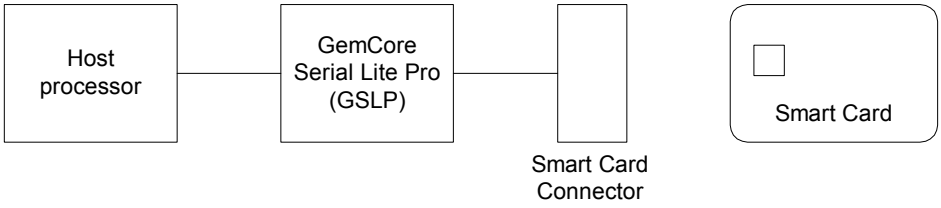

Figure 1 - Basic Architecture of a Smart Card Reader

The connection with the host processor is achieved via a serial asynchronous link; the rate can be selected from a range from 1200 to 115,200 bps.

The software inside the GemCore chip handles a communication protocol with the host system called the Gemplus Block Protocol (GBP).

A GBP Interface Library Kit can be provided, upon request. It consists of the source code of the GBP communication layer between the host and GemCore. It is written in the C language. See the Gemplus developers' site at **www.gemplus.com**.

Smart Card Interface

Compliance with Standards	• ISO/IEC 7816-1, 2, 3 and 4 • EMV V96 • CB • Mondex, Proton,ZKA, other: contact Gemplus
Supported Smart Cards	• Number of smart cards supported = 1 • Asynchronous cards, T=0, T=1 • Synchronous/memory cards using a command interpreter • EMV or non-EMV cards
Transmission Speed	• 9.6 Kbps to 115 Kbps
Electrical Interface	• Card power supply: 1.8V/3V/5V • ESD protection on card pins: 4 KV - human body model • Card presence or insertion detection • Short circuit current limitation

Host Interface

Physical Layer	• Serial asynchronous link • Programmable transmission speed from 1,200 bps to 115,200 bps • Format: 8 bits, no parity, 1 stop bit • Adjustable signal voltage
Protocol	• Gemplus Block Protocol (GBP) • GBP Interface Library Kit source code

Chip Power Supply

Voltage	• VCC: 2.85 V to 5.4 V
Consumption	• 8 mA typical • 150 mA max - smart card powered
Power Down Mode	• 100 µA max power down current • Power down/Power up by host command

Additional Features

Temperature Range	• Operating range: 0°C to +70°C • Extended operating range: contact Gemplus • Storage: -65°C to +150°C
Package	• 24 pins (SS0P24-type)
LED Management	• The LED is on when the card is powered on

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Pin Description

Pinout

The following figure shows the GemCore Serial Lite PRO 24-pin SSOP pinout:

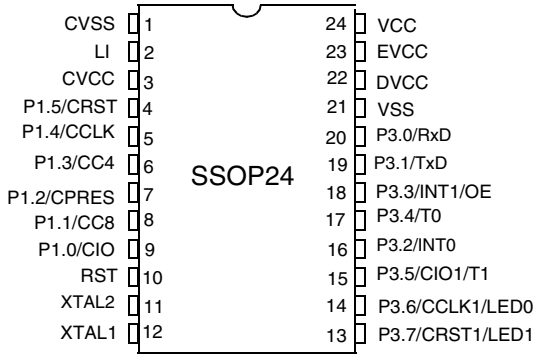

Figure 2 - GemCore Serial Lite PRO 24-pin SSOP Pinout

Signals

Port	Signal Name	Internal Power Supply	ESD	Type	Description
P1.0	CIO	CV_{CC}	4KV	I/O	Smart card interface function Card I/O - Pull-up medium must be <20 KΩ
P1.1	CC8	CV_{CC}	4KV	I/O	Smart card interface function Card contact 8 - Pull-up medium must be < 20KΩ
P1.2	CPRES	V_{CC}	4KV	I	Smart card interface function Card presence
P1.3	CC4	CV_{CC}	4KV	I/O	Smart card interface function Card contact 4 - Pull-up medium must be < 20KΩ

Table 1 - Description of the Pins

Port	Signal Name	Internal Power Supply	ESD	Type	Description
P1.4	CCLK	CV_{CC}	4KV	O	Smart card interface function Card clock
P1.5	CRST	CV_{CC}	4KV	O	Smart card interface function Card reset - Pull-up medium must be $<20K\Omega$
P3.0	RxD	EV_{CC}		I	UART function Receive data input
P3.1	TxD	EV_{CC}		O	UART function Transmit data output
P3.2	INT0	DV_{CC}		I/O	Input/Output function P3.2 is a bidirectional I/O port with internal pull-ups.
P3.3	INT1	EV_{CC}		I/O	Input/Output function P3.3 is a bidirectional I/O port with internal pull-ups.
P3.4		EV_{CC}		I/O	Input/Output function P3.4 is a bidirectional I/O port with internal pull-ups.
P3.5	CIO1	DV_{CC}		I/O	Input/Output function P3.5 is a bidirectional I/O port with internal pull-ups.
P3.6	CCLK1	DV_{CC}		O	LED function These pins can be directly connected to the cathode of the standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
P3.7	CRST1	DV_{CC}		I/O	Input/Output function P3.7 is a bidirectional I/O port with internal pull-ups.
RST		V_{CC}		I/O	Reset Input Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, regardless of whether the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and V_{SS}. Asserting $\overline{RST}$ when the chip is in Idle mode or Power-Down mode returns the chip to normal operation. The output is active for at least 12 oscillator periods when an internal reset occurs.

Table 1 - Description of the Pins

Port	Signal Name	Internal Power Supply	ESD	Type	Description
XTAL1		V_{CC}		I	Input to the on-chip inverting oscillator amplifier To use the internal oscillator, a crystal/ resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.
XTAL2		V_{CC}		O	Output of the on-chip inverting oscillator amplifier To use the internal oscillator, a crystal/ resonator circuit is connected to this pin. If an external oscillator is used, XTAL2 may be left unconnected.
VCC				PWR	Supply Voltage V_{CC} is used to power the internal voltage regulators and internal I/Os.
LI				PWR	DC/DC Input LI must be tied to V_{CC} through an external coil (typically 4,7 µH) and provide the current for the pump charge of the DC/DC converter.
CVCC				PWR	Card Supply Voltage CV_{CC} is the programmable voltage output for the card interface. It must be connected to an external decoupling capacitor.
DVCC				PWR	Digital Supply Voltage DV_{CC} is used to supply the digital core and internal I/O's. It is internally connected to the output of a 3 V voltage regulator and must be connected to an external decoupling capacitor.
EVCC		V_{CC}		PWR	Extra Supply Voltage EV_{CC} is used to supply the level shifters of UART interface I/O pins. It must be connected to an external decoupling capacitor.
CVSS				GND	DC/DC Ground CV_{SS} is used to sink high shunt currents from the external coil.
VSS				GND	Ground

Table 1 - Description of the Pins

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Electrical Characteristics

Absolute Maximum Ratings

Ambient Temperature Under Bias	-25°C to +85°C	Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. This value is based on the maximum allowable die temperature and the thermal resistance of the package.
Storage Temperature	-65°C to + 150°C	
Voltage on V_{CC} to V_{SS}	-0.5 V to + 6.0 V	
Voltage on Any Pin to V_{SS}	-0.5 V to V_{CC} + 0.5 V	

DC Parameters

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 2.85V to 5.4V; F=7.36MHz to 16MHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input high voltage except XTAL1, $\overline{RST}$	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input high voltage, XTAL1, $\overline{RST}$	0.7 V_{CC}		V_{CC} + 0.5	V	
DI_{CC}	Digital supply output current	10			mA	C_L = 100 nF F = 16 MHz x 1
DV_{CC}	Digital supply voltage	2.65	2.9	3.0	V	C_L = 100 nF
V_{PFDP}	Power fail high level threshold		2.55		V	
V_{PFDM}	Power fail low level threshold		2.45		V	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1µs		600	second	

Table 2 - Core DC Parameters (XTAL, $\overline{RST}$)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	-0.5		0.4	V	
V_{IH}	Input high voltage	0.7 x EV_{CC}	EV_{CC}	$EV_{CC + 0.5}$	V	External EV_{CC} mode
V_{OL}	Output low voltage			0.4	V	I_{OL} = 1.2 mA
V_{OH}	Output high voltage	0.8 x EV_{CC}		EV_{CC}	V	External EV_{CC} mode
EI_{CC}	Extra supply current			+3	mA	C_L = 100 nF
EV_{CC}	Extra supply voltage	1.6		V_{CC}	V	External EV_{CC} mode

Table 3 - Serial Interface DC Parameters (P3.0, P3.1, P3.3 and P3.4)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output low current, P3.6	2	4	8	mA	

Table 4 - LED Outputs DC Parameters (P3.6)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card supply current	60		121 105 102	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card supply voltage	4.6		5.4	V	I_{CARD} = 55mA

Table 5 - Smart Card 5V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card supply current	60		110 89 110	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card supply voltage	2.76		3.24	V	I_{CARD} = 60mA

Table 6 - Smart Card 3V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card supply current	20		109 100 82	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card supply voltage	1.68		1.92	V	I_{CARD} = 20mA

Table 7 - Smart Card 1.8V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output low voltage	0 0		$0.2xCV_{CC}$ 0.4	V	I_{OL} = 20µA (1.8,3V) I_{OL} = 50µA (5V)
I_{OL}	Output low current			15	mA	
V_{OH}	Output high voltage	$0.7xCV_{CC}$ $0.7xCV_{CC}$ CV_{CC}-0.5		CV_{CC} CV_{CC} CV_{CC}	V V V	I_{OH} = 20µA (1.8V) I_{OH} = 20µA (3V) I_{OH} = 50µA (5V)
I_{OH}	Output high current			15	mA	
$t_R t_F$	Rise and fall delays			8%xT 22.5 50	ns	C_{IN} = 30pF (5V) C_{IN} = 30pF (3V) C_{IN} = 30pF (1.8V)
	Voltage stability	-0.25 CV_{CC}-0.5		$0.4xCV_{CC}$ CV_{CC}+0.25	VV	Low level High level

Table 8 - Smart Card Clock DC Parameters (Port 1.4)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IIL}	Input low voltage	0 0		0.5 0.15xCV_{CC} 0.4	V	I_{IL} = 500µA I_{IL} = 20µA
I_{IL}	Input low current			500	µA	
V_{IH}	Input high voltage	0.7xCV_{CC}		CV_{CC}	V	I_{IH} = -20µA
I_{IH}	Input high current			-20/+20	µA	
V_{OL}	Output low voltage	0		0.4 0.4 0.3	V	I_{OL} =1mA (5V) I_{OL} =1mA (3V) I_{OL} =1mA (1.8V)
I_{OL}	Output low current			15	mA	
V_{OH}	Output high voltage	0.8xCV_{CC}		CV_{CC}	V	I_{OH} = 20µA (5V, 3V, 1.8V)
I_{OH}	Output high current			15	mA	
$t_R t_F$	Rise and fall delays			0.8	µs	C_{IN} = 30pF output

Table 9 - Smart Card I/O DC Parameters (P1.0)

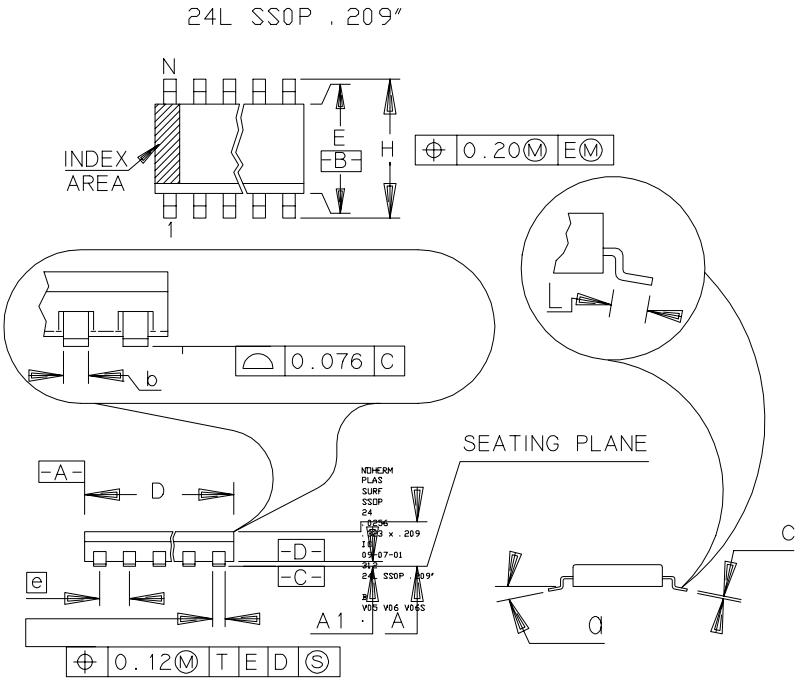
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output low voltage	0 0		0.2xCV_{CC} 0.4	V	I_{OL} = 20µA I_{OL} = 50µA
I_{OL}	Output low current			15	mA	
V_{OH}	Output high voltage	CV_{CC} - 0.5 0.8 x CV_{CC}		CV_{CC}	V	I_{OH} = 50µA I_{OH} = 20µA
I_{OH}	Output high current			15	mA	
$t_R t_F$	Rise and fall delays	0		0.8	µs	C_{IN} = 30pF
	Voltage stability	-0.25 CV_{CC} -0.5		0.4xCV_{CC} CV_{CC} + 0.25		Low level High level

Table 10 - Smart Card RST, CC4, CC8, DC Parameters (Port 1.5, P1.3, P1.1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{OL1}	CPRES weak pull-up output current	3	10	25	µA	P1.2=1, short to V_{SS}

Table 11 - Card Presence DC Parameters (P1.2)

Mechanical Data



	MM		INCH	
A	1.73	1.99	.068	.078
A1	0.05	0.21	.002	.008
b	0.25	0.38	.010	.015
C	0.09	0.20	.004	.008
D	8.07	8.33	.318	.328
E	5.20	5.38	.205	.212
e	0.65	BSC	.0256	BSC
H	7.65	7.90	.301	.311
L	0.63	0.95	.025	.037
N	24		24	
Q	0°	8°	0°	8°

Figure 3 - Mechanical Data

B

Electrical Schematic

PCB Design Considerations

Rep	Qty	Description		Reference Part		Package	Manufacturer AVL
C1	1	Ceramic Capacitor SMD	10%	100nF	25 V	0603	
C2	1	Ceramic Capacitor SMD	GRM42-6X5R475K10	4.7µF	10V	1206	Murata
C3	1	Ceramic Capacitor SMD	GRM42-6X5R475K10	4.7µF	10V	1206	Murata
C4	1	Ceramic Capacitor SMD	10%	470pF	25V	0603	
C5	1	Ceramic Capacitor SMD	10%	22pF	25V	0603	
K1	1	Smart card connector		SF1W010S1A			JAE
D1	1	LED 3mA				0805	
L1	1	Inductor SMD 4.7µH		LQH3C4R7M34		1210	Murata
Q1	1	Resonator ceramic SMD	14.74 MHz	CSTCV14.74MXJ040			Murata
U1	1	Microcontroller		GemCore Serial Lite PRO		SSOP24	Gemplus
R1	0	Resistor 1/10W	5%	0R		0603	
C6	01	Ceramic Capacitor SMD	10%	82pF	25V	0603	

Table 12 - Part List

The R1 resistor is reserved for future use. It should not be mounted but its tracks must be present in case of future necessity. All tracks should be as short as possible. The GND should be designed as a ground plane.

C4 and C5 should be as close as possible to the smart card connector to reduce noise and interference.

R1, C1, C2, C3, L1 and Q1 should be close to U1.

For EMVCo certification, the smart card connector must be equipped with a smart card detection switch. The switch must be closed when the smart card is present in the connector.

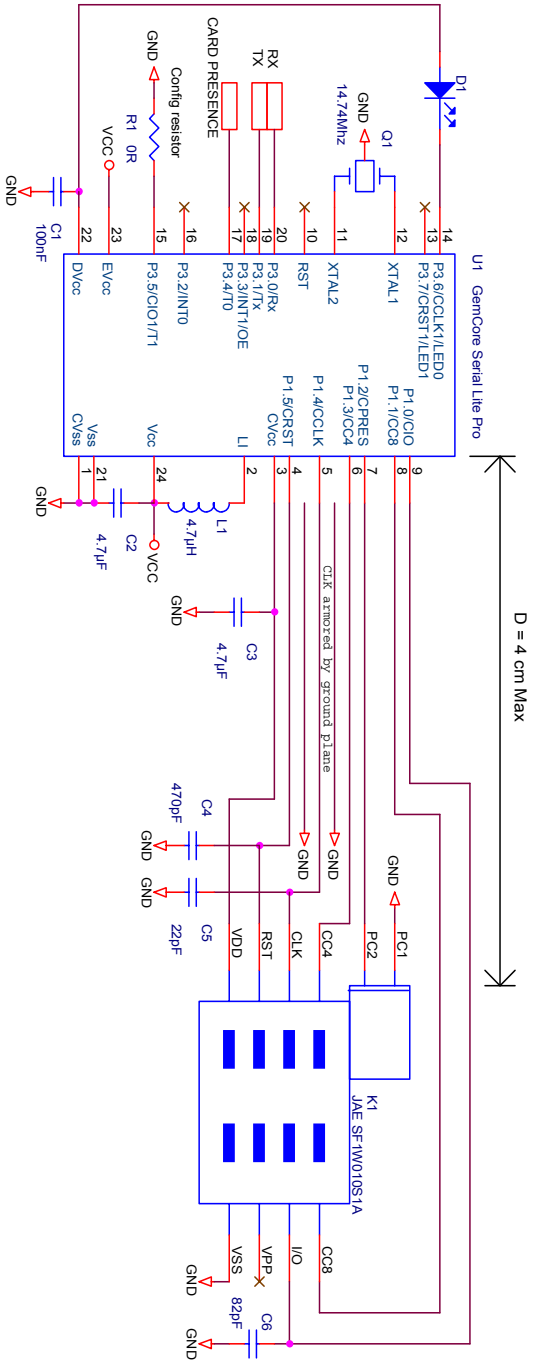


Figure 4 - Electrical Schematic

Note: The R1 resistor is not mounted and it is reserved for future use.

For More Information

For additional information about GemCore Serial Lite PRO, refer to the following documents:

Standards and Specifications

- *ISO 7816 standard, parts 1, 2, 3 and 4.*

Recommended Reading

- *GemCore Serial Lite PRO V1.4 Reference Manual*
- *GBP Interface Library Kit Programmer's Guide*
- *GemCore-Based Reader Testing Guidelines*

Terminology

Abbreviations

bps	Bits per second
GBP	Gemplus Block Protocol
GSLP	GemCore Serial Lite PRO
ISO	International Standards Organization
LED	Light Emitting Diode